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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,707	02/13/2004	Ryohei Nishimiya	1075.1245	5698

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EXAMINER	
LEE, CHUN KUAN	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 10/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,707	NISHIMIYA, RYOHEI	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
10/6/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/09/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection. Further more, applicant's arguments have been fully considered but they are not persuasive. Claim rejections of claims 1-4 under 35 U.S.C. 112 second paragraph is withdrawn. Currently, claims 1-5 are pending for examination.

2. In responding to applicant's argument regarding independent claim 1 rejected under 35 U.S.C. 102(b) that the Osaka reference is not applicable to the claimed limitations of independent claim 1 because the objective of Osaka's invention differs from the applicant's invention, such as no noise will occur on the bus as the noise is suppressed, as stated on page 5, last paragraph to page 7, 3rd paragraph. Applicant's arguments have fully been considered, but are found not to persuasive.

Applicant's arguments appears to state that the Osaka reference is nonanalogous art, please note that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Osaka reference teaches the suppression of the glitch noise that occurs on bus line (bus line of Fig. 1) at the time of active-line insertion of the

device unit, wherein such suppression is implemented by computing the noise propagation timing, and the computed noise propagation timing is associated with all device units that are currently actively connected on said bus line. Further more, Osaka does teach the insertion of glitch noise on the bus line because the suppression of the glitch noise will completely prevent the insertion of any glitch noise, but rather, reduces the glitch noise inserted to a small amount that would be acceptable without causing malfunction to the system (Osaka, col. 8, l. 24 to col. 9, l. 7 and col. 14, ll. 4-38).

3. In responding to applicant's argument regarding independent claim 1 rejected under 35 U.S.C. 102(b) that the Osaka reference does not teaches the shifting of the glitch noise which is resulted from insertion/withdrawal of the device unit, as stated on page 8, ll. 12-16. Applicant's arguments have fully been considered, but are found not to be persuasive.

Please note that the features upon which applicant relies on does not appear to be recited in the amended independent claim 1. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Further more, Osaka reference teaches the delaying of the switch control signal (Fig. 9, ref. 42) by Δt, thus delaying the connection of the device unit to the bus line, as the result, the glitch noise is shifted by the delaying of the switch control signal which connects the device unit to the bus line.

4. In responding to applicant's argument regarding independent claims 4-5 rejected under 35 U.S.C. 103(a) that it would not have been obvious for the Osaka reference to further include time "f" during which the glitch noise propagate to device units of other systems and clock skew "g" of each of the device unit, as stated on page 9, 2nd paragraph. Applicant's arguments have fully been considered, but are found not to be persuasive.

Please note that the independent claims 4-5 are rejected under 35 U.S.C. 103(a). Osaka teaches the generation of the glitch noise after the bus switch shifts from off to on or on to off and the propagation of said glitch noise which may result in the potential malfunction causing the apparatus connected to the bus line to function incorrectly (Osaka, col. 8, l. 22 to col. 9, l. 7), therefore the propagation of said glitch noise in the device unit and the bus line would have the propagation delay time of "f." Osaka further teaches the skewing of the clock in the system (Osaka, col. 14, ll. 4-10), wherein the clock skew is well known to one skilled in the art as the delay of the clock signal from the source where the clock signal originated to the desired destination, therefore the clock skew from the source where the clock signal originated to the other one of said plurality of device unites or the other device connected on the bus line would be "g." As in the previous office action, Osaka teaches that the sum of the value of DELTAt (i.e. "b"), switching time T_{pzh} of the switch element (i.e. "d"), propagation delay of the switch signaling (i.e. "c") and a clock skew of the system (i.e. "a") is smaller than the bus-clock cycle time T_{clk} (i.e. "T") (Osaka, col. 14, ll. 4-7), which results in $b + d + c + a < T$ which equates to

$0 < T - (a + b + c + d) = M$ (time marginal); and

It would then be obvious to further include into "M" the variables such as the delay time "f" and the skew "g" for the desire to further optimize "M," which is consistent with the analysis set forth by MPEP 2144.05 under Optimization of Ranges, wherein the inclusion of "f" would reduce the likelihood of the glitch noise causing malfunction in the system and the inclusion of "g" would provide more accurate estimation of "M" and loosing the timing requirement for "b." The following computation is reiterated the previous office action, wherein the pulse width (time) "e" and the setup time "S" are also included and utilizing the similar derivation as discussed above:

$T > (a + b + c + d) + (e + f) - g + S$

$T > b + (a + c + d) + (e + f) - g + S$

$b < T - [\,(a + c + d) + (e + f) - g + S\,]$

$0 < T - [\,(a + c + d) + (e + f) - g + S\,] - b = T - (a + c + d + e + f) + g - S - b = M$

$M = (T + g) - (a + b + c + d + e + f) - S > 0.$

5. As per claims 2-3, dependent claims 2-3 are unpatentable at least due to dependency on the rejected independent claim 1.

6. In responding to all applicant's arguments, the examiner reiterates his rejections of claims 1-5 in detail below.

Terminal Disclaimer

7. The terminal disclaimer filed on 08/09/2006 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of any patent granted on Application Number 11/317011 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Osaka et al. (US Patent 5,787,261).

9. As per claim 1, Osaka teaches a design method for a bus system equipped with

a plurality of device units (Fig. 1; Fig. 10, ref. 141, 142 and col. 16, ll. 36-63),

a data bus on which said plurality of device units are connectible (Fig. 10, ref. 201, 202, 211, 212 and Bus Lines of Fig. 1);

a timing-signal supply source supplying a timing signal to said plurality of device units through a timing-signal bus (clock line transmitting a clock signal, wherein the clock signal is provided by the back panel 5 of Fig. 1 and col. 12, l. 45 to col. 13, l. 7),

a bus switch connecting and disconnecting a signal between said plurality of device units and said data bus (Fig. 1, ref 11); and

a bus-switch control part controlling the connecting and disconnecting operations of said bus switch (Fig. 1 ref. 14);

said design method comprising:

computing, for each of said plurality of device units, based on a cycle of said timing signal (clock signal from the back panel; col. 12, l. 61 to col. 13, l. 8), a signal propagation delay in each one of said plurality of device units (propagation delay of the switch control signal; col. 14, ll. 4-38), signal propagation delays in said timing-signal bus (clock skew; col. 14, ll. 4-38) and said data bus (inherent signal skew similar to the clock skew would be present for the data bus), and a setup time in another one of said plurality of device units (the amount of time for the functional circuit board to stabilize after the functional circuit board is connected and powered; col. 6, l. 65 to col. 7, l. 12) or another device connected on said data bus, timing at which, when each one of said plurality of device units is connected on said data bus being active, noise propagates (propagation of glitch noise; col. 8, ll. 22-38 and col. 8, l. 60 to col. 9, l. 7) to the other one of said plurality of device units or to the other device connected on said data bus (col. 6, l. 65 to col. 9, l. 7 and col. 12, l. 45 to col. 14, l. 38); and

computing, based on said computed timing, connection timing at which each one of said plurality of device units is connected on said data bus (col. 14, ll. 4-38), wherein the connection time is the delay DELTAt amount of time and then each one of said plurality of device units is connected to the data bus (col. 6, l. 65 to col. 9, l. 7 and col. 12, l. 45 to col. 14, l. 38).

10. As per claim 2, Osaka teaches the design method for a bus system further comprising wherein in said computing, based on said computed timing, said connection

timing is computed by computing a delay time "b" (Δt 50 of Fig. 8) needed for said bus switch to connect each one of said plurality of device units on said data bus after each one of said plurality of device units is connected on said timing-signal bus (col. 13, l. 8 to col. 14, l. 38).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osaka et al. (US Patent 5,787,261).

Osaka teaches design method for a bus system, comprising:

a plurality of device units connectible to a printed circuit board (Fig. 1; Fig. 10, ref. 141, 142 and col. 16, ll. 36-63), wherein the back panel to which the plurality of device units is connectible to is couple to the printed circuit board (such as the motherboard);

a data bus on which said plurality of device units are connectible (Fig. 10, ref. 201, 202, 211, 212 and Bus Lines of Fig. 1);

a timing-signal supply source supplying a timing signal to said plurality of device units through a timing-signal bus (clock line transmitting a clock signal, wherein the clock signal is provided by the back panel 5 of Fig. 1 and col. 12, l. 61 to col. 13, l. 7),

a bus switch connecting and disconnecting a signal between said plurality of device units and said data bus (Fig. 1, ref 11); and

a bus-switch control part controlling the connecting and disconnecting operations of said bus switch (Fig. 1 ref. 14);

wherein said bus-switch control part controls said bus switch so that each one of said plurality of device units is connected on said data bus after a delay time "b" (Δt_{50} of Fig. 8) of said bus switch from connection of each one of said plurality of device units with said timing-signal bus (col. 13, l. 8 to col. 14, l. 38),

generating the glitch noise after the bus-switch is shift from off to on or on to off and the propagation of said glitch noise resulting in the potential malfunction causing the apparatus connected to the bus lines to function incorrectly (col. 8, l. 22 to col. 9, l. 7), wherein the glitch noise would comprise a pulse width (time) "e" and a propagation delay time "f";

setup time "S" in said bus system (col. 6, l. 65 to col. 7, l. 5), wherein setup time is the amount of time require for the functional circuit board to become stabilized after connecting to the bus line and power supplied,

the generation and distribution of a clock signal within the system, comprising the skew of the clock signal from the source to the associated functional blocks (col. 12, l. 61 to col. 13, l. 7 and col. 14, ll. 4-38);

and wherein, based on cycle "T" of said timing signal (T_{clk}) (col. 14, ll. 4-38),

skew "a" from said timing-signal supply source to said bus switch control part (clock skew of the system) (col. 14, ll. 4-38), wherein the clock skew of the clock signal

from the source of the clock signal to the desired destination is inherent to the system, therefore, the clock skew from the source of the clock signal to another one of said plurality of device unit or the other device connected on said data bus would be skew "g",

the delay time "b" of said bus switch (Δt or DELTAt) (col. 14, ll. 4-38),

signal propagation delay time "c" between said bus switch control part and said bus switch (propagation delay time of the switch control signal traveling to the switch) (col. 14, ll. 4-38),

operating delay time "d" of said bus switch (switch time T_{pzh}) (col. 14, ll. 4-38),

the delay time "b" of said bus switch is computed as such:

$T > b + (a + c + d)$ (wherein the sum of the value of DELTAt, switching time T_{pzh} of the switch element, propagation delay of the switch signaling and a clock skew of the system is smaller than the bus-clock cycle time T_{clk} ;col. 14, ll. 4-38);

therefore $b < T - (a + c + d)$; and

the resulting time margin is $M = T - (a + c + d) - b = T - (a + b + c + d) - b > 0$, wherein M is 0 or greater.

Osaka teaches the plurality of variables comprising the pulse width (time) "e," the propagation delay time "f," the skew "g" and the setup time "S," (as stated above) but does not expressly teach that the computation of the value M utilizing the above plurality of variables, resulting in the computation of $M = (T + g) - (a + b + c + d + e + f) - S$.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include the plurality of parameters comprising the pulse width

(time) "e," the propagation delay time "f," the skew "g" and the setup time "S," into the determination of M, therefore further optimize the time margin M, consisting with the analysis set forth in MPEP 2144.05 under Optimization of Ranges. The resulting equation of time margin would then be

$T > b + (a + c + d) + (e + f) - g + S;$

$b < T - ((a + c + d) + (e + f) - g + S) = (T + g) - (a + c + d + e + f) - S;$

$0 < (T + g) - (a + c + d + e + f) - S - b = (T + g) - (a + b + c + d + e + f) - S = M;$

therefore $M = (T + g) - (a + b + c + d + e + f) - S > 0;$

wherein by including the parameters of "e" and "f," the computer system can ensure that glitch noise will never cause malfunction resulting in the apparatus to function incorrectly;

wherein by including the parameter "g", the propagation delay of the clock signal to the rest the apparatus other than current connected functional block (Fig. 1, ref. 3), the time margin M can be increased, therefore loosing the timing requirement for "b"; and

wherein it would be obvious to include the setup time "S" as it is required every time for the functional circuit board to stabilize after connecting to the data bus and powering up before shifting the bus switch from off to on, connecting the functional circuit board to the bus lines, and causing the glitch noise.

Therefore, it would have been obvious to one skilled in the art to include the plurality of parameters comprising the pulse width (time) "e," the propagation delay time

"f," the skew "g" and the setup time "S," into the determination of M for the benefit of higher signal integrity for a hot plugging system and method.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C.K.L
10/03/2006

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